What is claimed is:

1. A method for forming a semiconductor device comprising:

providing a structure of a semiconductive material with a hardmask thereover, said hardmask having at least one tapered portion with a corresponding portion of a further film disposed thereover;

etching an uncovered portion of said hardmask to expose an exposed portion of said semiconductive material while maintaining said at least one tapered portion and each said corresponding portion substantially intact; and

etching said exposed portion of said semiconductive material while maintaining said at least one tapered portion and each said corresponding portion substantially intact.

2. The method as in claim 1, wherein said providing comprises providing said hardmask with an originally tapered upper surface covered by said further film, and removing a first portion of said originally tapered upper surface and a first portion of said further film to produce said hardmask having said at least one tapered portion with a corresponding portion of said further film disposed thereover, and said uncovered portion.

3. The method as in claim 2, wherein said removing comprises chemical mechanical polishing.

4. The method as in claim 2, wherein said further film comprises an oxide liner and said removing includes forming a spacer oxide material over said further film and etching portions of said spacer oxide material and said first portion of said further film.

5. The method as in claim 4, wherein said removing further includes, after said etching said portions of spacer oxide material and said first portion, forming an etch stop layer thereover and an interlevel dielectric over said etch stop layer, then planarizing such that said uncovered portion of said hardmask is planarized.

6. The method as in claim 1, wherein said further film comprises an oxide film.

7. The method as in claim 6, wherein said etching an uncovered portion of said hardmask includes a hardmask:further film etch selectivity ranging from 5:1 to 10:1.

8. The method as in claim 1, wherein said semiconductive material comprises polycrystalline silicon.

9. The method as in claim 1, wherein, after said etching said exposed portion of said semiconductive material, removing said at least one tapered portion with a corresponding portion of a further film disposed thereover, thereby producing at least one corresponding gate structure of said semiconductive material.

10. The method as in claim 9, wherein each of said at least one corresponding gate structure includes a width of about 10 nanometers.

11. The method as in claim 1, wherein said structure of a semiconductive material includes a width within the range of 50 to 500 nanometers.

12. The method as in claim 1, wherein said etching said subjacent portion of said semiconductive material includes a semiconductive material:hardmask etch selectivity ranging from 50:1 to 100:1.

13. The method as in claim 1, wherein said hardmask is formed of SiN or SiON.

14. The method as claim 1, wherein said providing includes providing a layer of material of said hardmask over a semiconductor substrate surface and etching to produce said hardmask having at least one tapered portion, each tapered portion having a taper angle within the range of 45° to 85° with respect to said semiconductor substrate surface.

15. A method for forming a semiconductor device comprising:

providing a layer of hardmask material over a semiconductor substrate;

forming a photoresist pattern over said layer of hardmask material;

etching to produce a discrete portion of said hardmask material, said discrete portion having at least one tapered section with a taper angle within the range of 45° to 85° with respect to a surface of said semiconductor substrate;

carrying out a photoresist strip process;

forming an oxide layer over said discrete portion;

removing portions of said oxide layer and planarizing to produce said discrete portion having a substantially planar uncovered portion and each tapered section having a corresponding portion of said oxide layer thereover.

16. The method as in claim 15, in which said etching includes at least one etchant species chosen from the group consisting of CF_4, CHF_3, CH_2F_2, CH_3F, C_5F_8, CO, Ar, and O_2.

17. A semiconductor device comprising a semiconductive material formed over a substrate, having a width no greater than 10 nm and a top surface substantially parallel to said substrate, a hardmask formed on said top surface and having an angled upper surface and an oxide film formed thereover, said angled upper surface and said top surface forming an angle ranging from 45° to 85°.

18. The semiconductor device as in claim 17, wherein said semiconductive material comprises polysilicon.

19. The semiconductor device as in claim 18, wherein said hardmask is formed of SiN or SiON.

20. A semiconductor device comprising a discrete semiconductive material structure formed over a substrate surface and having a top surface substantially parallel to said substrate surface, said structure including at least one masked portion having a hardmask formed on said top surface, said hardmask having an angled upper surface

and an oxide film formed thereover, said angled upper surface and said top surface forming an angle ranging from 45° to 85°.

21. The semiconductor device as in claim 1, wherein said hardmask is formed of SiN or SiON.

22. The semiconductor device as in claim 1, wherein said at least one masked portion comprises a duality of said masked portions disposed at opposed ends of said discrete semiconductive material structure.